Simulation Methodology and Evaluation of Through Silicon Via (TSV)-FinFET Noise Coupling in 3-D Integrated Circuits

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***Abstract*— Bulk FinFETs have emerged as the solution to short-channel effects at the 22-nm technology node and beyond. The capability of 3-D stacking of dies from various technologies will eventually enable stacking FinFET dies within 3-D integrated circuits. Within 3-D circuits, through silicon vias (TSVs) are a known source of substrate noise in planar bulk technologies. While FinFETs are expected to demonstrate superior noise immunity relative to planar devices due to superior gate control over and volume inversion of the active fin, the impact of TSV noise on FinFETs has not been previously quantified. To evaluate TSV-FinFET noise coupling, we develop in this paper a simulation methodology that extends the state of the art by accurately modeling substrate noise due to digital signals on nearby TSVs and improving the extraction of substrate circuit models from full-wave electromagnetic simulations. To overcome the lack of high-fidelity FinFET SPICE models that accurately capture the effects of substrate noise, we use high-fidelity technology computer-aided design (TCAD) FinFET models. Our results show that FinFETs exhibit an order of magnitude less leakage current noise transients, and two orders of magnitude less saturation current noise transients, relative to comparable planar technologies. Our findings are generalizable, showing that FinFETs are significantly more robust to substrate noise than equivalent planar devices.**

***Index Terms*— 3-D integrated circuit (IC), computer-aided design (CAD), through silicon via (TSV).**

I. Introduction

FINFETS have emerged as the solution to short-channel effects (SCEs) at the 22-nm technology node and beyond [1]. Intel is currently producing integrated circuits (ICs) using bulk trigate FinFET devices incorporating rounded corners, work function engineering, channel strain engineering, and fin body doping [2]. FinFETs have superior immunity to SCEs relative to planar [3], and it is anticipated that FinFETs will enable technology scaling beyond technology nodes achievable with planar devices [4].

By integrating dies from various technologies, 3-D die stacking offers unique opportunities to create high-performance (HP) systems, characterized by low power, low latency, high bandwidth, and small form factor. FinFETs are poised to contribute to such systems. One 3-D integration concern is the impact of through silicon vias (TSVs) on neighboring devices. Noise from TSV signals couple to transistors through the TSV oxide liner and the bulk substrate.

Prior investigations have reported a wide range (3–92 mV) of TSV-induced substrate noise in planar bulk processes [5], [6]. While TSV noise can be mitigated using various technologies such as guard rings, increased liner thickness, and ground plugs [7], characterizing TSV noise for new technologies to ensure proper circuit operation remains a necessity.

We address in this paper the impact of 3-D TSV noise on FinFET devices. One challenge for analyzing TSV noise is properly accounting for the variable capacitance of the metal–oxide–semiconductor capacitor (MOS-C) formed by the TSV metal plug, oxide liner, and the bulk substrate [8]. Our novel approach is to extract a model of the variable capacitance using the Synopsys Technology Computer Aided Design (TCAD) device simulator [9]. Our proposed MOS-C extraction technique accurately captures the effects of complex physical phenomena such as trapped charges in the oxide liner and supports large signal noise analysis appropriate for analyzing noise due to digital signals on the TSV. Another challenge is measuring the TSV noise induced at the substrate contact of a transistor. Full-wave and quasi-static electromagnetic (EM) computer-aided design (CAD) tools model the electrical propagation and potentials between the conductors, respectively. However, the substrate contact of the transistor is a location in the lossy bulk dielectric. We develop in this paper a method for extracting equivalent impedances between the TSV and the transistor substrate contract using a combination of the Q3-D Extractor 3-D parasitic solver [10] and the high frequency structural simulator (HFSS) full-wave EM solver [11], both from ANSYS. One final challenge is simulating the impact of TSV-induced substrate noise on FinFET performance without accurate SPICE models. Eventually, common multigate compact models from the Berkeley BSIM-CMG project [12] will be suitable for analyzing the noise impact on FinFETs. However, there are currently no open source FinFET process design kits (PDKs) and existing models have known limitations for modeling the body effect. Therefore, we use a high-fidelity TCAD FinFET device model [13] in our methodology. We simulate comparable 22-nm planar transistors using predictive technology models (PTMs), Level 54 BSIM 4.0 SPICE models [14], from Arizona State University [15], [16].

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We apply our methodology to evaluate the impact of noise from TSV digital signals on FinFET performance and we compare the noise immunity of FinFETs with conventional planar transistors. The major contributions of our work are as follows.

1) We developed a generalized methodology for evaluating the effect of noise on a transistor output due to digital transitions on nearby TSVs, properly modeling all three critical interfaces (i.e., TSV oxide liner, the lossy substrate, and the active device).
2) We extracted the first large-signal simulation model for a TSV MOS-C that captures complex phenomena such as trapped charges in the oxide liner.
3) We developed an improved accuracy RF substrate model extraction technique based on full-wave and quasi-static EM solvers.
4) We performed the first comparative analysis of TSV noise impact on FinFET and conventional planar transistors.
5) We showed improved noise robustness of FinFETs over planar devices. This finding is generalizable to noise sources other than TSVs.

This paper is organized as follows. In Section II, we review the prior modeling of the TSV MOS-C and substrate noise coupling between TSVs and active devices. In Section III, we describe our generalized methodology for evaluating transistor performance impact due to TSV digital signal-induced noise coupling. In Section IV, we compare the impact of TSV noise coupling on FinFETs with conventional planar transistors. We conclude our work in Section V with a short summary and proposed future work.

II. Prior Work

A. Modeling the TSV MOS-C

The first analytical description of the TSV MOS-C was reported in [17]. Bandyopadhyay *et al.* calculated the MOS-C using the full depletion approximation in cylindrical coordinates, identifying power distribution network (PDN) noise coupling has high-frequency MOS-C characteristics while signal distribution network (SDN) noise-coupling has deep-depletion MOS-C characteristics. Cho *et al.* [18] reported measurements demonstrating duty cycle distortion in TSV-to-substrate noise coupling due to the nonlinear MOS-C, highlighting the need to properly model the TSV MOS-C for noise coupling analysis.

Katti *et al.* [19] developed an analytical model for estimating the signal delay through a TSV, including considerations for fixed charges in the oxide liner, and verified the model with device simulation. Cadix *et al.* [20] developed an analytical model including the charge density at the SiO_2/Si interface. The approaches of [19] and [20] are not optimal for SDN noise coupling, because they do not model the MOS-C in deep depletion.

Recently, Chen *et al.* [21] developed a compact TSV model amenable to time-domain SDN simulation considering time and voltage dependencies. The work focused on the signal propagation through the TSV, not TSV-substrate noise coupling. The authors based the model on [19], adding additional model components to support the time-varying deep-depletion and quasi-static behaviors. The model is based on the full-depletion approximation, does not support fixed charges in the oxide, and is not verified with device simulation. Our methodology is novel because we extract a TSV MOS-C model that accurately captures complex physical phenomena, such as trapped charges in the oxide liner, and is suitable for large-signal, time-domain analysis of noise coupling to nearby transistors.

B. Methodologies for Evaluating 3-D Noise Coupling

Prior methodologies for evaluating 3-D noise coupling through the substrate use quasi-static device simulation, transmission line matrix (TLM) method, and EM solvers. Trivedi and Mukhopadhyay [22] performed a quasi-static simulation of through oxide vias in silicon on insulator (SOI) using TCAD. Because their analysis was specific to SoI they did not include TSV MOS-C effects. Duan *et al.* [23] used a full-wave EM finite element method solver, a 3-D TLM, and equivalent circuit models to compare noise coupling between bulk and SoI. The authors identified a reduction in noise coupling for SoI due to the isolation provided by the buried oxide, but their model also omits TSV MOS-C effects.

Brocard *et al.* [24] performed EM and device co-simulation using DevEM. This approach captures both the EM noise propagation through the substrate and the semiconductor MOS-C effects, although DevEM does not provide support for simulating fixed charges at the SiO_2/Si interface. However, their work did not include the characterization of substrate noise found at the transistor substrate contact. Le Maitre *et al.* [25] used DevEM to extract a frequency dependent, compact TSV model of the path between the TSV, and a conductive substrate contact. We adopt the circuit structure of their extracted models and extend their work to extract a model of the coupling between the TSV and the transistor substrate contact.

Xu *et al.* [26] developed compact models based on an analytical approach for electrical coupling between a TSV and nearby transistors. The models include small-signal TSV MOS-C effects and have been validated with a full-wave EM solver. These models were developed for the analysis of PDN noise—not SDN noise—therefore assuming static boundary conditions derived from a fixed TSV bias voltage. We extend their EM simulation methodology to support analysis of SDN noise, introducing additional modifications to improve accuracy. Their HFSS extraction was performed with lumped ports between a nonphysical observation point (OP) and a nearby ground. While the introduction of the OP solves the problem of extracting EM coupling to a location in the lossy dielectric, the presence of the OP skews the fields. Also, lumped ports in HFSS artificially constrain the magnitude and orientation of the incident EM fields, introducing additional error. Ideally, the fields only depend on the material properties and geometry of the physical structures in the circuit. A description of our extraction improvements can be found in Section III-B.

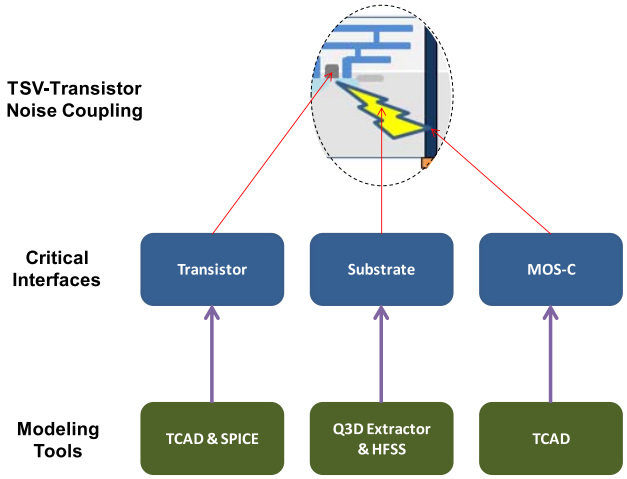

Fig. 1. Generalized methodology to simulate the impact of TSV digital signal noise on nearby transistors.

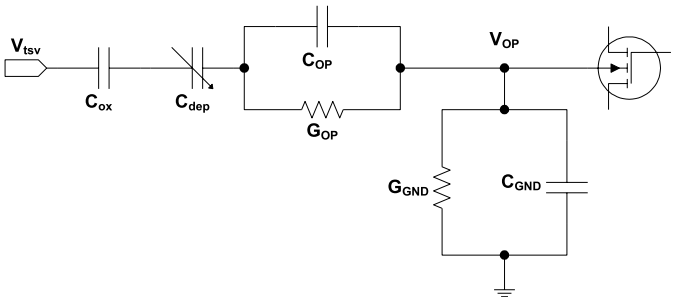

Fig. 2. Schematic representation of the noise coupling from TSV digital signals to the transistor substrate contact. Frequency-parameterized discrete elements are used to capture the coupling through the TSV liner and the substrate. SPICE or TCAD device models are used to simulate the noise impact on transistor performance.

III. Generalized Methodology for Evaluating Transistor Performance Due to Nearby TSV Signal Coupling

We propose a time-domain simulation methodology to evaluate the impact of nearby TSV signals on transistor performance. Our methodology combines models for each of the three critical interfaces shown in Fig. 1.

First, we use TCAD to extract the large-signal MOS-C model due to the combined oxide capacitance and depletion region capacitance formed by the TSV. Second, we extract a ground-referenced model for the substrate impedance between the TSV and the transistor body using Q3-D Extractor and HFSS. Finally, we use TCAD and compact models to determine the noise impact on FinFET and planar transistor performance, respectively. The three models (TSV, substrate, and transistor) are combined into a SPICE circuit netlist (Fig. 2) to evaluate the impact of TSV digital signals on nearby FinFET and planar transistors.

A. TSV MOS-C Model Extraction

Digital signals couple from the TSV to the bulk substrate through the oxide liner. The MOS interface formed by the TSV (Fig. 3) creates a MOS-C, and the resulting capacitor

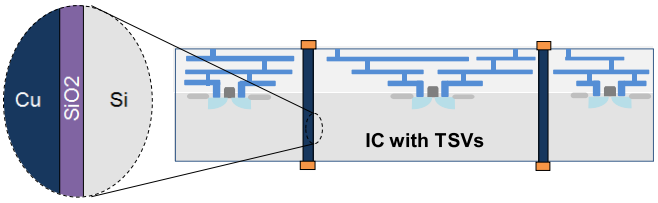

Fig. 3. TSV MOS-C formed by the TSV metal plug, oxide liner, and the bulk silicon substrate.

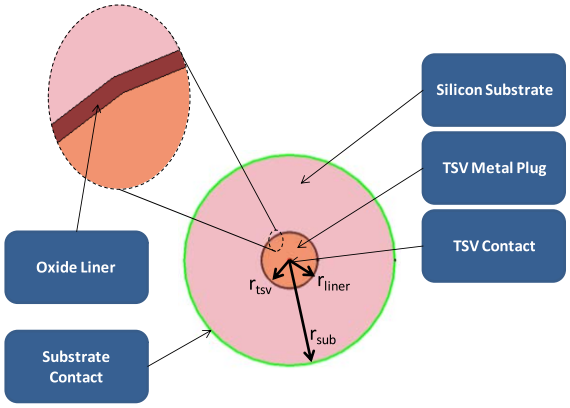

Fig. 4. TCAD TSV model cross section for extracting MOS-C deep-depletion characteristics from a particular TSV geometry.

is the combination of the oxide capacitance and the bias-dependent depletion region capacitance. Digital signals on the TSV generate a MOS-C with deep-depletion characteristics.

We extract the MOS-C CV curves using the Synopsys TCAD package. We define a 2-D TSV model (Fig. 4) with geometries from [27]: a Cu metal plug of radius $r_{\text{tsv}} = 2.6\ \mu$m, an 120-nm thick SiO_2 liner with radius $r_{\text{liner}} = 2.72\ \mu$m, and a substrate larger than the maximum depletion region width under deep depletion ($r_{\text{sub}} = 10\ \mu$m). The substrate is p-type with a boron doping concentration of 10^{15} cm^{-3}. The TSV is driven by a 0.1-μm radial contact from the center of the copper plug and the substrate contact is located at the edge of the substrate region. A mesh is generated with maximum edge length of 25 nm at the Si/SiO_2 interface.

We define three fixed oxide charge density concentrations at the Si/SiO_2 interface: a baseline value of 7.8×10^{11} cm^{-2}, as found in [27]; -8.43×10^{11} cm^{-2}, corresponding to the proposal in [28] for controlling the MOS-C over the intended TSV operating voltage range; and 0.63×10^{11} cm^{-2}, a moderate charge density between the two other values. The simulated TSV height is 20 μm corresponding to the measured TSV structure in [27].

We capture the deep-depletion characteristics of the TSV MOS-C for each of the three fixed oxide charge density concentrations by applying a piecewise linear ramp from -10 to $+10$ V to the TSV contact with a rise time of 1 V/μs, connect the substrate contact to ground, and extract the current flowing between the TSV and substrate. At this ramp rate, substrate parasitics are negligible—substrate parasitics are extracted separately in the following section. The CV curves are calculated from the simulation output by applying the

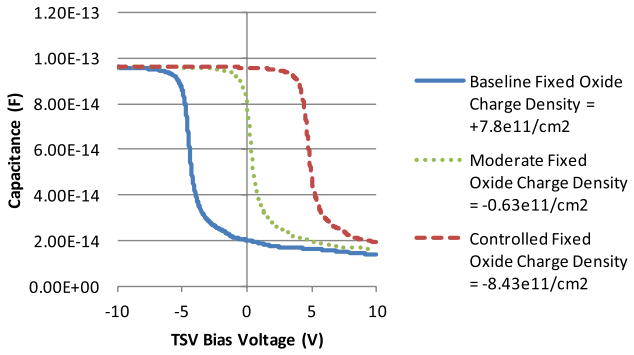

Fig. 5. TSV CV curves with different fixed charge interface densities. Capacitance values include both the fixed liner capacitance and the deep-depletion MOS-C capacitance.

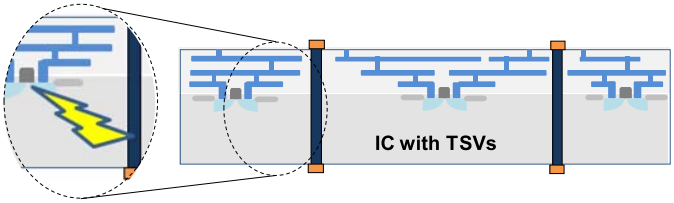

Fig. 6. Notional noise coupling path from the TSV to the transistor through the bulk silicon substrate. Noise propagates through the substrate volume, not on the active top surface.

formula: $C(V) = I/(dV/dt)$. The extracted TSV MOS-C is compactly modeled in SPICE with a voltage-dependent current source, the HSPICE G-element, with the voltage controlled capacitor (VCCAP) keyword selected. The variable capacitor is specified with a piecewise linear lookup table using the CV data extracted from the TCAD simulation. The TSV node provides the voltage input to the MOS-C VCCAP G-element, capturing the bias dependence of the MOS-C in HSPICE. The TSV extraction simulation takes 12 969 cpu-s on a Dell PowerEdge R815 with 4, 12-core 2.3-GHz AMD Opteron 6176 processors, and 128 GB of memory.

The results are shown in Fig. 5. The extracted data from our model compares favorably with previously reported measured capacitance data [27], [28]. The baseline MOS-C is in deep depletion within the operating range 0–0.7 V, and therefore changes slowly over this range. The controlled fixed oxide charge density MOS-C is accumulated over the operating range, and therefore is roughly constant over this range, although at the greater value of C_{ox}. The moderate fixed oxide charge density MOS-C is in the depletion region in the 0–0.7 V operating range, and therefore experiences the greatest capacitance shift; we will use this value in the following simulations to demonstrate effects of the nonlinear capacitance.

B. Substrate Coupling Extraction

Noise couples from the TSV into the substrate and propagates through the IC (Fig. 6). Consider a digital edge propagating through the TSV with a rise time of $t_r = 50$ ps; the bandwidth of this signal is approximately $0.35/t_r = 7$ GHz, corresponding to a wavelength of 12.5 mm in silicon.

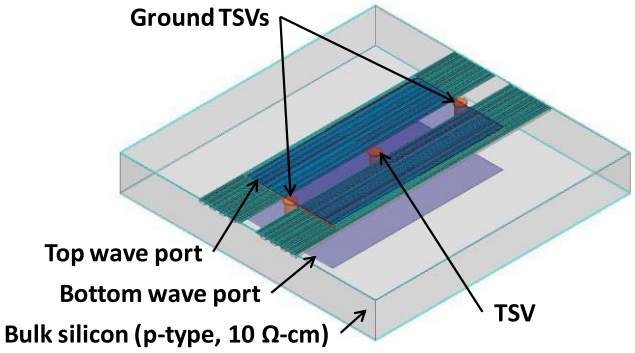

Fig. 7. Simple TSV substrate model with V_{ss} and V_{dd} shorted together for high-frequency substrate extraction. The two additional TSVs (top and bottom) tied to the PDN provide the ground reference for the wave ports.

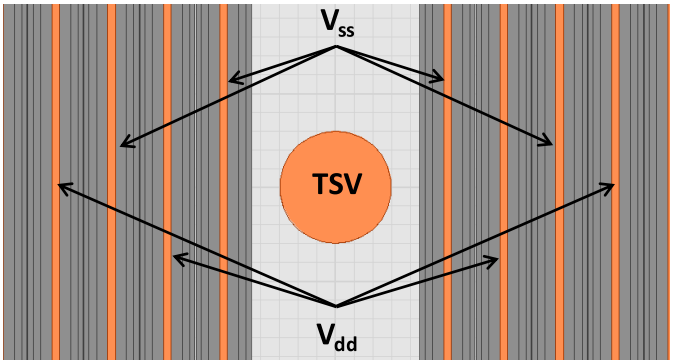

Fig. 8. Simple TSV substrate model (top view) with regular PDN topology of alternating V_{ss} and V_{dd} traces.

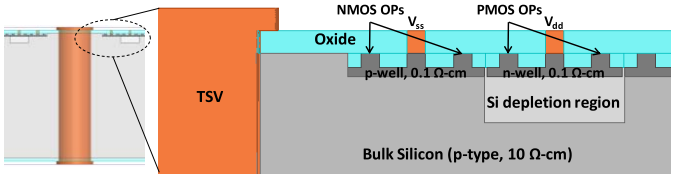

Fig. 9. Simple TSV substrate model. Left: front view. Right: detail. Transistors are placed in a regular layout with alternating nMOS and pMOS distributed between the PDN traces.

The distances to nearby metal features and transistors are less than 1/10 this minimum wavelength, therefore quasi-static analysis is sufficient to capture the EM coupling from the TSV to the PDN. However, using modern CAD tools to extract a substrate equivalent circuit model is deceivingly complex. Quasi-static field solvers (Q3D Extractor) are designed to extract metal-to-metal coupling; full-wave EM solvers (HFSS) do not extract lumped impedance values.

We require a ground-referenced equivalent circuit model to an OP in the substrate dielectric below the transistor channel (V_{OP}, Fig. 2). Because the OP is neither a physical structure in the design nor a conductor, the extraction is not directly supported using either HFSS or Q3D. We circumvent this limitation with a three step process applied to the CMOS layout from [29] (Figs. 7–9). The height of the TSV is 20 μm, the keep out zone between the TSV and the center of the

nearest nMOS transistor is 2.4 μm, and the V_{ss}/V_{dd} lines alternate every 3 μm. The nMOS and pMOS OPs are located directly under the channel of the left-most transistor site where the callouts terminate in Fig. 9.

Step 1: Extract the total admittance Y_{TOT} based on the capacitance and conductance between the TSV and the PDN (V_{ss} and V_{dd}) using Q3D. Because only high-frequencies propagate through the TSV liner and MOS-C, we short V_{ss} and V_{dd} together in the model and perform small-signal RF analysis on the substrate—large signal effects are limited to the MOS-C extracted in the previous section. We define our substrate materials and geometries to match the model used in [29]. We omit the oxide and TSV MOS-C depletion capacitances from our substrate extraction—these capacitances were determined in Section III-A and will be composed with the substrate model in Section IV. The simulation is driven with a source on the bottom TSV pad and a sink on the top TSV pad. Capacitance and conductance matrices are extracted over frequency from 0.01 to 100.01 GHz in 1-GHz steps.

Step 2: Extract the potential at the OP due to the coupling between the TSV and the PDN using HFSS. We simulate the same circuit in HFSS, saving the E-field over the same frequency range. This simulation is driven with a 1 V excitation using a wave port at the bottom pad of the TSV and terminated with a wave port at the top pad of the TSV. Both wave ports are referenced to ground at the ground TSVs shown in Fig. 7. The simulated structure is encapsulated in a radiation boundary box. The OP potential is extracted relative to the nearby V_{SS} using the field calculator to integrate the electric field over a line from V_{ss} to the OP: $V_{OP} = \int_l \vec{E} \cdot \vec{dl}$.

Step 3: Apportion the total admittance between the TSV–OP and the OP $-$ V_{ss}, as shown in Fig. 2. For each frequency point, convert the total admittance (Y_{TOT}) to equivalent impedance (Z_{TOT}), divide the total impedance between $Z_{OP} = (1 - V_{OP})Z_{TOT}$ and the $Z_{GND} = V_{OP} \cdot Z_{TOT}$ based on the complex potential at the OP, and convert the two resulting impedances back to admittances Y_{OP} and Y_{GND}. The extracted frequency-dependent admittances are included in the SPICE simulation using S-element models in HSPICE with the TYPE set to Y-parameters. The frequency-dependent admittances are captured with small-signal parameter data frequency table models (SP models).

The extracted models run much faster (0.21 cpu-s) than the initial Q3D extraction (44 393 cpu-s) and HFSS extraction (30 149 cpu-s).

Our substrate extraction methodology eliminates two sources of error found in [7] and [26]. We compare our extraction methodology with the prior art by simulating the same model in HFSS first with a physical OP, a copper cube with 0.1-μm per side, and then using lumped ports for extraction. Whereas we extract the OP voltage by calculating the line integral of the electric field, previous approaches calculated the OP voltage using the Z-parameters extracted from the lumped port: $V_{OP} = Z_{21}/Z_{11}$. However, lumped ports are only appropriate for use with fields aligned to the port geometry. The lumped port introduces extraction error ranging from a fractional percent at low frequency to over 6% at 100 GHz (Fig. 10). Previous approaches introduced additional

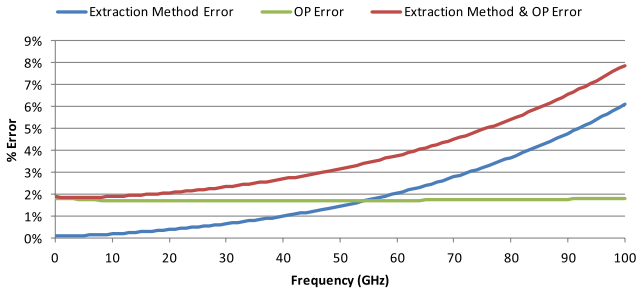

Fig. 10. Substrate extraction error due to (a) use of lumped ports and (b) inclusion of a physical OP, compared with our proposed extraction technique.

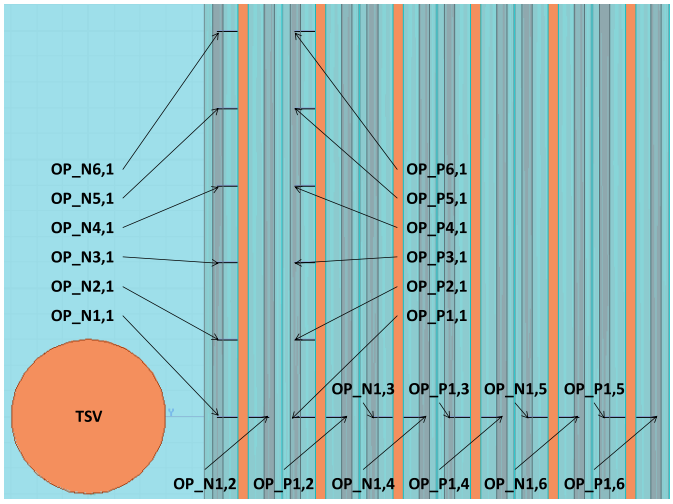

Fig. 11. Simple TSV substrate model (top view) with multiple OPs.

error over the entire frequency range by modeling the OP as a metallic cube. A physical OP shunts the electric field over the OP surface, changing the potential at the extraction point. The combined error ranges from 1.9% at low frequency to 7.9% at 100 GHz (Fig. 10) for an OP with 0.1-μm per side. Our proposed extraction technique is fully generalizable for impedance extraction to an arbitrary OP in a dielectric so long as the fields are quasi-static for the geometry under evaluation.

Noise propagation through the substrate is a function of distance between the TSV and the OP at the transistor body. Fig. 11 shows a top view of the substrate model with OPs instantiated along the first column and row of nMOS and pMOS transistors relative to the TSV center. The OPs are named OP_(N/P)R, C where (N/P) identifies nMOS or pMOS, R identifies the row number, and C identifies the column number. The rows are each spaced 3 μm in the vertical direction, starting parallel to the TSV center. The first nMOS column is 5 μm from the TSV center in the horizontal. The column distance between each pair of nMOS or pMOS OPs is 2 μm and the column distance between consecutive nMOS/pMOS OPs is 1 μm. The lines shown between V_{dd}/V_{ss} and the OPs are the lines of integration used to calculate the potential at each OP as described in the procedure above.

The noise attenuation between the TSV and the OP increases as the distance increases, and decreases as the frequency increases (Figs. 12–15). The pMOS OPs show

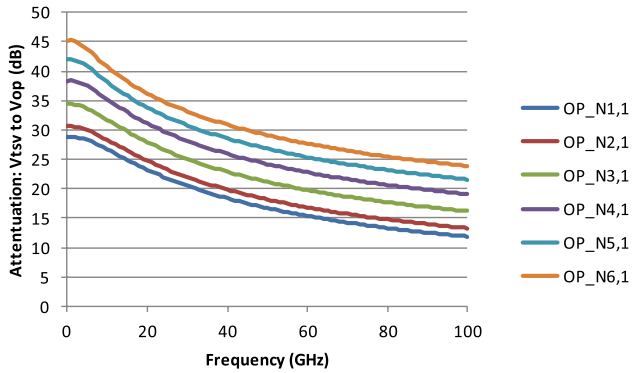

Fig. 12. Noise attenuation versus frequency (nMOS, column).

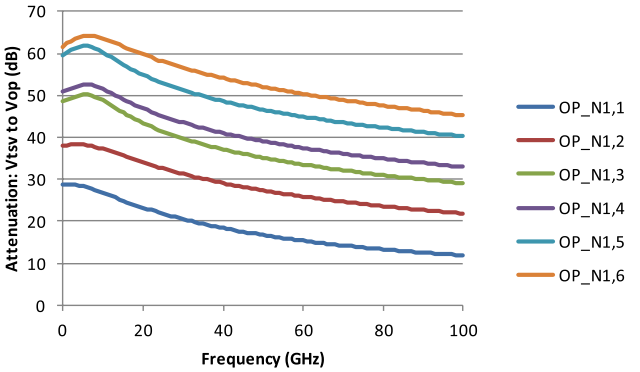

Fig. 13. Noise attenuation versus frequency (nMOS, row).

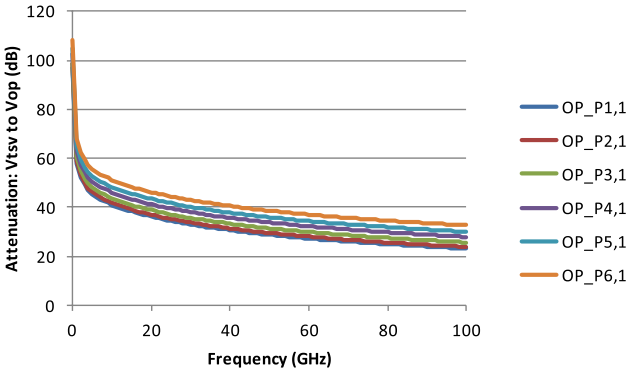

Fig. 14. Noise attenuation versus frequency (pMOS, column).

significant attenuation at low frequencies due to the depletion region formed between the n-well and the substrate; however, the pMOS depletion region provides only modest attenuation above 5 GHz. The benefit is minimal when we consider the TSV liner capacitance from the previous section, which provides an excellent low-frequency isolation for both nMOS and pMOS. The distance down the columns provides greater noise attenuation than the distance down the rows due to the isolation provided by the vertical V_{ss}/V_{dd} lines.

C. FinFET and Planar Transistor Modeling

Substrate noise at the transistor body impacts transistor performance via the body effect and capacitive coupling through the transistor (Fig. 16). These phenomena are well characterized for planar transistors. We use the PTM HP

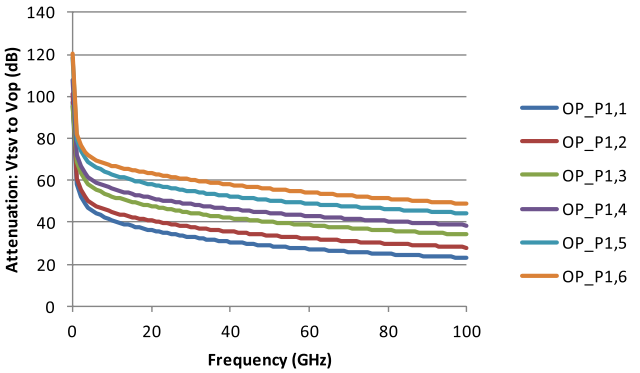

Fig. 15. Noise attenuation versus frequency (pMOS, row).

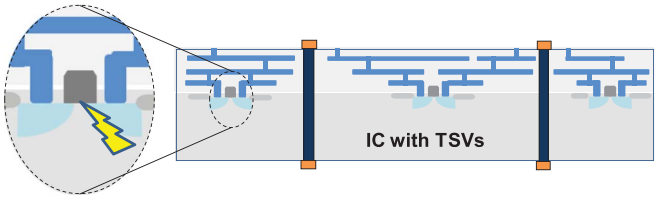

Fig. 16. TSV-induced substrate noise impacts the transistor via the substrate contact.

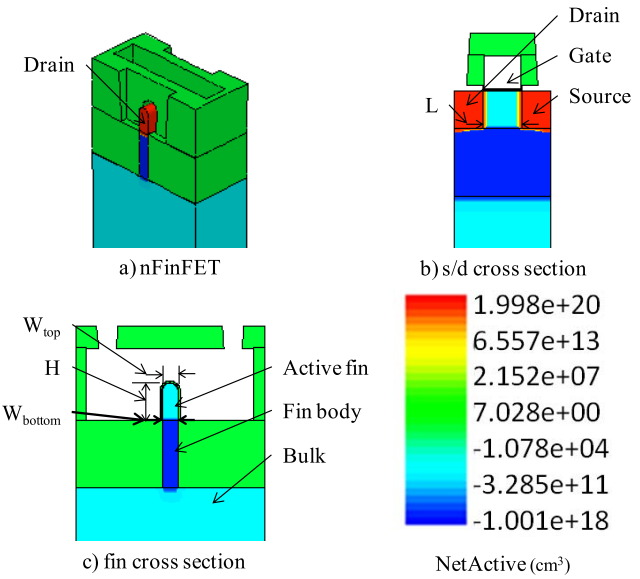

Fig. 17. Doping concentration of nFinFET structure. (a) Isomorphic view. (b) Source/drain cross section cut at middle of fin. (c) Fin cross section cut at middle of channel.

Version 2.1 SPICE models from Arizona State University to evaluate the impact of TSV-induced substrate noise on planar transistors in the 22-nm technology node [15], [16]. Our PTM simulations use an nMOS transistor with $L = 34$ nm and $W = 72.0$–78.6 nm to match the gate length and effective width, respectively, of the FinFET in Fig. 17.

The impact of substrate noise is not well characterized for FinFETs. The BSIM CMG SPICE models include experimental body effect modeling beginning with version 106.0.0; however, these empirical models have known limitations and there are no open source PDKs available that accurately capture the body effect for FinFET. Therefore, we use a TCAD

TABLE I
nFinFET MODEL GEOMETRY PARAMETERS

Parameter	Description	Value
L	Gate length	34 nm
H	Fin height	35 nm
W_{bottom}	Width of the bottom of the active fin	15 nm
W_{top}	Width of the top of the active fin	7 nm

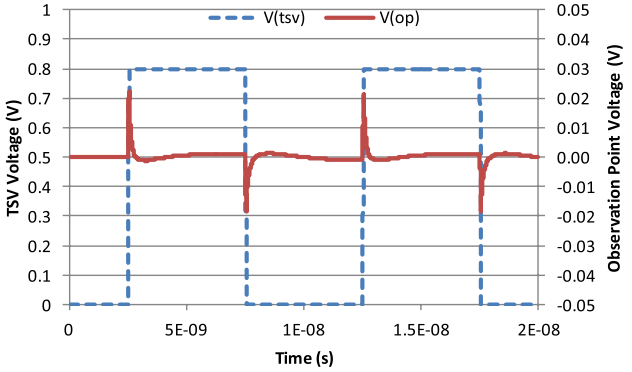

Fig. 18. Transient voltage noise observed at OP_N1_1 due to a digital signal transition on the nearby TSV.

FinFET model to compare the substrate noise immunity of FinFET with planar technology.

We base our analysis on the 22-nm bulk nFinFET TCAD model (Fig. 17) adapted from [13]. This model represents the transistor features described in [2]. The key geometries shown in Table I have been selected to correspond with Intel's recent bulk FinFET production process [30]. The active fin is undoped with a p-type concentration of 10^{15} cm^{-3}, and the fin body is doped with a p-type concentration of 10^{18} cm^{-3}. The corner radius of the rounded fin is set to 1/2 W_{top} to minimize corner effects. We also evaluate the impact of fin shape on noise susceptibility; therefore, we evaluate W_{top} from 1 to 15 nm. All other model parameters take the default value. The simulations include physical models for stress effects, crystal orientation-dependent quantum effects, band-to-band-tunneling, and drift-diffusion with mobility degradation.

IV. TSV NOISE COUPLING COMPARISON: FinFET VERSUS PLANAR

We combine the extracted models for the TSV and the substrate in SPICE with PTM and TCAD transistor models to evaluate the TSV-induced noise immunity of FinFETs relative to planar. The SPICE netlist for the FinFET models are run within the mixed-mode TCAD environment.

We first simulate the TSV and substrate models to determine the TSV voltage noise observed at the closest OP. We observe from Fig. 18 that a simulation input waveform, V_{tsv}, of a 0.8 V digital signal on the TSV with 50-ps rise (fall) time imparts a transient voltage noise, V_{OP}, of 22.3 mV (-18.9 mV) reported for OP_N1_1.

Next, we evaluate the impact of a steady-state substrate voltage bias on the transistor output via the body effect. We simulate W_{top} from 1 to 15 nm (2-nm step) to explore the impact of fin shape on the body effect. We apply a bias

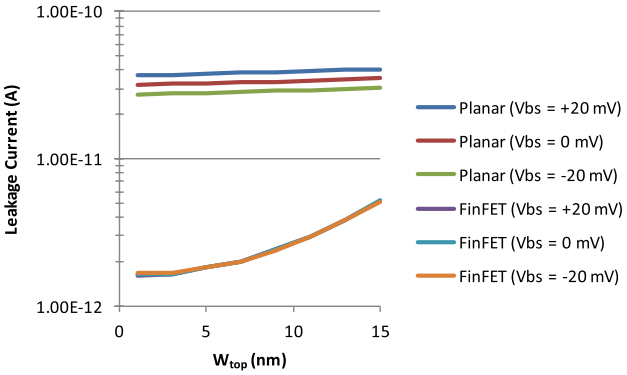

Fig. 19. Impact of substrate bias on leakage current for planar and FinFET. For all planar configurations, W_{eff} is set to the effective width corresponding to a FinFET with W_{top}.

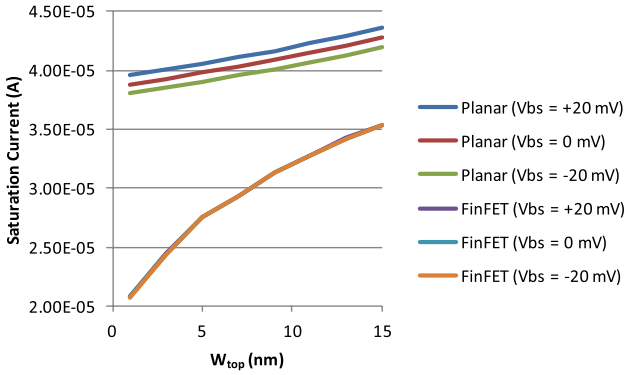

Fig. 20. Impact of substrate noise on saturation current for planar and FinFET. For all planar configurations, W_{eff} is set to the effective width corresponding to a FinFET with W_{top}.

of $\pm$20 mV to each transistor configuration, comparable with the worst case V_{OP}.

The FinFET leakage exhibits a significant dependence on fin shape, but the change in leakage due to the body effect is negligible for all fin shapes with the $\pm$20-mV substrate bias (Fig. 19). The same substrate bias on the planar transistor induces a $+16\%/-14\%$ change in leakage current. Similarly, while the FinFET saturation current exhibits a significant dependence on fin shape, the change in saturation current due to the body effect is negligible for all fin shapes (Fig. 20). The same substrate bias on the planar transistor induces a $\pm 1.9\%$ change in saturation current.

Finally, we evaluate the impact of the transient TSV-induced substrate noise on FinFET and planar transistors. Here, we only simulate the FinFET with the default $W_{\text{top}} = 7$ nm, comparable with modern production devices. We simulate each transistor with the substrate noise from the first 10 ns of Fig. 18, with the transistor biased off ($V_g = 0$ V) from 0 to 5 ns and on ($Vg = 0.8$ V) from 5 to 10 ns. The TSV-induced substrate noise voltage results in current transients with three orders of magnitude increase from a reference leakage current of approximately 5×10^{-11} A for planar (top of Fig. 21). The FinFET leakage current transients exhibit two orders of magnitude increase relevant to a reference leakage current of approximately 2×10^{-12} A. Therefore, in addition to a reference leakage difference of one order of magnitude less

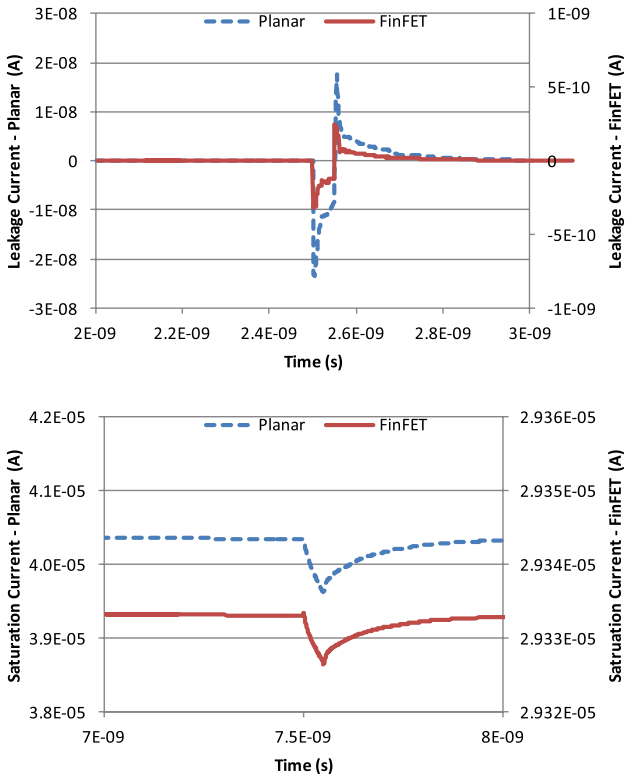

Fig. 21. Impact of transient TSV-induced substrate noise on leakage current (top) and saturation current (bottom) for FinFET and planar. FinFETs exhibit substantially improved immunity to substrate noise relative to comparable planar transistors.

than planar, the FinFET exhibits superior isolation to substrate noise when the transistor is off. The TSV-induced substrate noise voltage results in a 1.8% transient in the saturation current for planar from a reference current of 4.04×10^{-05} A (bottom of Fig. 21). The TSV-induced substrate noise voltage results in a 0.023% transient in the saturation current for FinFET from a reference current of 2.93×10^{-05} A. The FinFET therefore exhibits an improvement of two orders of magnitude over planar in terms of robustness of the saturation current to TSV noise.

The MOS-C extraction performed in Section III results in a more accurate assessment of the substrate noise relative to a fixed oxide capacitance alone. For the transient simulation (Fig. 20), using the fixed capacitance associated with the 0 V TSV bias results in over 7 mV of substrate noise error at the OP with significant ringing around the TSV digital transitions. This 7 mV change increases the peak transient leakage current by approximately 60% and the peak transient saturation current by approximately 0.5%. Modeling noise without our proposed accurate MOS-C extraction may impact simulation results for analog circuits.

V. Conclusion

We investigated in this paper the impact of TSV noise on nearby FinFETs. We developed a generalized methodology for evaluating the impact of TSV noise on nearby transistors that extends the state of the art. Our extracted MOS-C models enable substrate noise analysis due to digital signal transitions on nearby TSVs. Our TSV MOS-C model captures complex physical phenomena such as trapped charges in the oxide liner. We have shown that the typical fixed charge densities found in published TSV structures result in an order of magnitude change in TSV-substrate capacitance over the voltages found in typical digital circuits. We developed a substrate extraction procedure that measures electrical coupling to an OP in the lossy dielectric bulk substrate, with 2%–8% more accuracy at low–high frequencies than prior methods. Because we do not rely on physical OPs or lumped ports, our substrate extraction technique is more general than previous techniques, and can be applied in other situations when it is necessary to extract electrical coupling at a particular point within the substrate without altering the field distribution. The proposed work can be further enhanced and made easier for adoption for circuit simulation. Simulation results can be made more accurate using more realistic waveforms obtained through circuit simulation (e.g., a ring oscillator). Additionally, our work used an OP right below the transistor channel as the connecting point between the substrate and transistor simulation models. Planar and FinFET devices, however, have different detailed implementations in this interface between the channel and the substrate, which may have an impact on the extracted substrate coupling model. A more accurate approach is to model the specific details of FinFET and planar IC layouts in separate substrate models within HFSS.

We also performed the first comparative analysis of 3-D TSV noise impact on FinFET and conventional planar transistors. FinFETs exhibit an order of magnitude better leakage current noise immunity and two orders of magnitude better saturation current noise immunity relative to planar transistors. The findings regarding the increased noise robustness of FinFETs over planar devices are generalizable to noise sources other than TSVs. While the TSV-induced noise transients presented here are small in magnitude, they may be disruptive to sensitive analog circuit (e.g., amplifiers, phase-locked loop, and oscillator feedback loops). FinFETs exhibit superior substrate noise immunity over planar transistors, making them a strong candidate for future integration of system-on-chip analog circuits with TSVs.

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